UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,638	10/26/2001	Mark Wetzel	5150-51201	1406

7590 05/17/2004

Jeffrey C. Hood
Conley, Rose, & Tayon, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	3

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/014,638	WETZEL ET AL.
	Examiner	Art Unit
	Trisha U. Vu	2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/15/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-39 are presented for examination.

Specification

The disclosure is objected to because of the following informalities: "***bus lines 720***" (Specification, page 21, line 23) should be changed to "***bus lines 730***" to be consistent with Fig. 7. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8, 10-11, 13, 15, 17-26, and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over PXI Specification (Revision 1.0, August 20, 1997) (hereinafter PXI Spec) in view of InfiniBand Architecture Specification (Volume 1, Release 1.0, Oct 24, 2000) (hereinafter InfiniBand Spec).

As to claim 1, PXI Spec teaches an instrumentation system, comprising: a chassis (at least Figures 1.1, 2.2, 2.4, and 3.1), comprising: a plurality of slots (peripheral slots), wherein each of the plurality of slots is operable to receive an inserted module; a backplane (backplane), comprising: a plurality of instrumentation signaling lines which

provide instrumentation signaling functions (Figure 2.4); and a plurality of interface connectors coupled to the backplane, wherein each of the connectors is operable to connect to a respective inserted module; wherein the backplane is operable to provide for communication among the inserted modules (Section 2.1). However, PXI Spec does not explicitly disclose the backplane comprises a switch fabric bus. InfiniBand Spec teaches implementing switch fabric bus (InfiniBand) in backplane to provide communication between modules (at least Section 1.2, 1.3 and 13.2.6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement InfiniBand bus as taught by InfiniBand Spec in the system of Alappat to provide high speed communication between modules.

As to claim 2, InfiniBand Spec further teaches the switched fabric bus is a channel based switched fabric bus (IniniBand) (Specification).

As to claim 3, InfiniBand Spec further teaches the channel based switched fabric bus is the InfiniBand bus (Specification).

As to claim 4, InfiniBand Spec further teaches the switched fabric bus includes one or more routers and/or switches which are operable to selectively provide for communication between the inserted modules (at least Figure 2).

As to claim 5, PXI Spec further teaches the plurality of instrumentation signaling lines include: at least one local bus (Section 2.2.2 and Fig. 2.4), wherein the at least one local bus provides for adjacent slot communication for one or more of analog signals or digital signals (Section 2.2.2).

As to claim 6, PXI Spec further teaches the at least one local bus is operable to connect each of at least a subset of the plurality of slots with its adjacent slots, wherein the at least one local bus is operable to provide a communication path between the inserted modules for one or more of analog signals or side-band digital communications (Section 2.2.2)

As to claim 7, PXI Spec further teaches the plurality of instrumentation signaling lines includes one or more lines for transmitting one or more system reference clock signals (reference clock), wherein the one or more system reference clock signals are operable to provide synchronization signals for the inserted modules (Section 4.1.2.4).

As to claim 8, PXI Spec further teaches the reference clock signals are generated by a reference clock comprised on one or more of the backplane, one of the inserted modules, or an external system (external source) which is coupled to one of the inserted modules (Sections 4.1.2.4 and 4.1.2.5).

As to claim 10, PXI Spec further teaches the reference clock comprises a fixed frequency reference clock (PXI_CLK10) (Section 4.1.2.4).

As to claim 11, PXI Spec further teaches the reference clock comprises a variable frequency reference clock (Section 4.1.2.5).

As to claim 13, PXI Spec further teaches the plurality of instrumentation signaling lines include: a trigger bus, wherein the trigger bus comprises a plurality of trigger lines, wherein each of the plurality of trigger lines is operable to connect a respective one of the plurality of slots to the trigger bus, and wherein the trigger bus is operable to

communicate trigger signals between the inserted modules (Fig. 2.5 and Sections 2.2.4, 4.1.2.5).

As to claim 15, PXI Spec further teaches a star trigger controller slot, wherein the star trigger controller slot (star trigger/peripheral slot [2]) is operable to receive an inserted star trigger controller module (Section 2.2.5 and Fig. 2.4); wherein the plurality of instrumentation signaling lines include a star trigger bus, wherein the star trigger bus comprises a plurality of dedicated trigger lines, each connecting the star trigger controller slot to one of the plurality of slots (peripheral slots [3], [4],...), wherein the star trigger bus is operable to communicate precision trigger signals between the inserted star trigger controller module and in each of the inserted modules in the plurality of slots (Section 2.2.5 and Fig. 2.4).

As to claim 17, PXI Spec further teaches each of the dedicated trigger lines is of equal length to provide matched propagation times of the trigger signals (Section 2.2.5).

As to claim 18, PXI Spec further teaches the plurality of instrumentation signaling lines include a low voltage analog bus (Section 4.1.2.5).

As to claim 19, PXI Spec further teaches the plurality of instrumentation signaling lines include a high voltage analog bus (Section 4.1.2.5).

As to claim 20, PXI Spec further teaches the plurality of instrumentation signaling lines include one or more of: a local bus (Section 2.2.2); system reference clock signals (Section 2.2.3); a trigger bus (Section 2.2.4); and a star trigger bus (Section 2.2.5).

As to claim 21, PXI Spec further teaches the plurality of instrumentation signaling lines include two or more of: a local bus (Section 2.2.2); system reference clock signals (Section 2.2.3); a trigger bus (Section 2.2.4); and a star trigger bus (Section 2.2.5).

As to claim 22, PXI Spec further teaches the plurality of instrumentation signaling lines include three or more of: a local bus (Section 2.2.2); system reference clock signals (Section 2.2.3); a trigger bus (Section 2.2.4); and a star trigger bus (Section 2.2.5).

As to claim 23, PXI Spec further teaches the plurality of instrumentation signaling lines include two or more of: a local bus; system reference clock signals; a trigger bus; a star trigger bus; a low voltage analog bus; and a high voltage analog bus. (Sections 2.2.2-2.2.5 and 4.1.2.5).

As to claim 24, PXI Spec further teaches one or more instrumentation modules, wherein each of the one or more instrumentation modules is operable to be inserted into a respective one of the plurality of slots, wherein the backplane is operable to logically couple to each of the one or more instrumentation modules when inserted into the slots; wherein each of the one or more instrumentation modules is operable to perform instrumentation functions in the instrumentation system (Section 2.1 and Fig. 2.2).

As to claim 25, PXI Spec further teaches a system controller slot (system slot), wherein the system controller slot is operable to receive an inserted system controller module (system controller module), wherein the inserted system controller module is operable to provide system controller functions in the instrumentation system (Section 2.1 and Fig. 2.2).

As to claim 26, PXI Spec further teaches the system controller module comprises a computer module, wherein the computer module is operable to provide computer functions in the instrument9ation system (at least Section 5.4.2.1 and 5.5.3).

As to claim 29, PXI Spec does not explicitly disclose one or more chassis coupled to said chassis via a transmission medium. InfiniBand Spec further teaches coupling one or more chassis via a transmission medium (chassis-to-chassis) (Fig. 1 and Section 1.2.2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include coupling one or more chassis as taught by PXI Spec to provide the system expansion in the system of PXI Spec. PXI Spec as modified above by InfiniBand Spec further teaches each chassis comprising: a plurality of slots, wherein each of the plurality of slots is operable to receive an inserted module; a backplane, comprising: a switched fabric bus; and a plurality of instrumentation signaling lines which provide instrumentation signaling functions; a plurality of interface connectors coupled to the switched fabric bus and to the plurality of lines, wherein each of the connectors is operable to connect to a respective inserted module; wherein the backplane is operable to provide for communication among the inserted modules (as addressed above in claim 1).

As to claim 30, PXI Spec further teaches the plurality of signaling lines of said chassis are operable to transmit instrumentation signals through the transmission medium to said one or more additional chassis (InfiniBand Spec, Section 1.2.2), and wherein the plurality of instrumentation signaling lines of said one or more additional chassis are operable to provide the instrumentation signals to one or more inserted modules in said one or more additional chassis (PXI Spec, Section 2.2).

As to claim 31, PXI Spec further teaches said plurality of signaling lines of each of said chassis and said one or more additional chassis are operable to communicate instrumentation signals through the transmission medium with any others of said chassis and said one or more additional chassis, thereby providing for communication between inserted modules of any of said chassis and said one or more additional chassis (InfiniBand Spec, Section 1.2.2).

As to claim 32, InfiniBand Spec further teaches wherein the transmission medium comprises one or more transmission cables; and wherein said chassis and said one or more additional chassis are daisy-chained together by said one or more transmission cables, respectively (Section 3.4.1).

As to claim 33, InfiniBand Spec further teaches the transmission medium comprises a network (e.g. internet) (Chapter 3, page 54).

As to claim 34, InfiniBand Spec further teaches the network comprises the Internet (Chapter 3, page 54).

3. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over PXI Specification (Revision 1.0, August 20, 1997) (hereinafter PXI Spec) in view of InfiniBand Architecture Specification (Volume 1, Release 1.0, Oct 24, 2000) (hereinafter InfiniBand Spec), and further in view of Doblar et al. (US Pub. No. 2001/0013100) (hereinafter Doblar).

As to claim 9, the argument above for claim 8 applies. However, PXI Spec and InfiniBand Spec do not explicitly disclose the reference clock comprises a differential clock. Doblar teaches differential clock (at least paragraph [0011]). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to implement differential signal as taught by Doblar in the system of PXI Spec and InfiniBand to provide low power consumption and noise immunity.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over PXI Specification (Revision 1.0, August 20, 1997) (hereinafter PXI Spec) in view of InfiniBand Architecture Specification (Volume 1, Release 1.0, Oct 24, 2000) (hereinafter InfiniBand Spec), and further in view of Lee et al. (5,040,158) (hereinafter Lee).

As to claim 12, the argument above for claim 7 applies. However, PXI Spec and InfiniBand Spec do not explicitly disclose the reference clock signals are generated by two or more reference clocks comprises on one or more of the backplane, one of the inserted modules, or an external system which is coupled to one of the inserted modules. Lee teaches the reference clock signals are generated by two or more reference clocks comprised on one or more of the devices, or an external system which is coupled to one of the devices in the system (abstract and col. 2, lines 39-68). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include generating the system reference clock from other devices' reference clocks in the system as taught by Lee in the system of PXI Spec and InfiniBand Spec to determine a most appropriate reference clock of the system.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over PXI Specification (Revision 1.0, August 20, 1997) (hereinafter PXI Spec) in view of InfiniBand Architecture

Specification (Volume 1, Release 1.0, Oct 24, 2000) (hereinafter InfiniBand Spec), and further in view of Bell (6,356,140).

As to claim 14, the argument above for claim 13 applies. However, PXI Spec and InfiniBand Spec do not explicitly disclose the trigger bus comprise at least one open-collector signal line. Bell teaches open-collector line (col. 2, lines 30-48 and col. 5, lines 28-66). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include open collector signal line as taught by Bell in the system of PXI Spec and InfiniBand Spec to improve signaling speed.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over PXI Specification (Revision 1.0, August 20, 1997) (hereinafter PXI Spec) in view of InfiniBand Architecture Specification (Volume 1, Release 1.0, Oct 24, 2000) (hereinafter InfiniBand Spec), and further in view of Ohta (5,414,635).

As to claim 16, the argument above for claim 15 applies. However, PXI Spec and InfiniBand Spec do not explicitly disclose at least a subset of said dedicated trigger lines comprises one or more differential triggers. Ohta teaches differential triggers (at least col. 7, lines 5-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential triggers as taught by Ohta in the system of PXI Spec and InfiniBand Spec to provide low power consumption and noise immunity.

7. Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over PXI Specification (Revision 1.0, August 20, 1997) (hereinafter PXI Spec) in view of InfiniBand Architecture Specification (Volume 1, Release 1.0, Oct 24, 2000) (hereinafter InfiniBand Spec), and further in view of Shaffer et al. (6,349,286) (hereinafter Shaffer).

As to claim 27, the argument above for claim 25 applies. However, PXI Spec and InfiniBand Spec do not explicitly disclose the system controller module comprises an interface for coupling to an external system. Shaffer teaches interface for coupling to an external system (col. 6, lines 24-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement an interface for coupling to an external system as taught by Shaffer in the controller of PXI Spec and InfiniBand Spec to allow the system expansion.

As to claim 28, Shaffer further teaches the external system comprises a computer system (col. 6, lines 24-45).

8. Claims 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over InfiniBand Architecture Specification (Volume 1, Release 1.0, Oct 24, 2000) (hereinafter InfiniBand Spec) in view of PXI Specification (Revision 1.0, August 20, 1997) (hereinafter PXI Spec).

As to claim 35, InfiniBand Spec teaches a system, comprising: a computer system (e.g. Processor Node); a chassis (e.g. I/O chassis); a cable (InfiniBand) coupling the computer system and the chassis, wherein the cable transmits switched fabric bus signals (InfiniBand) between the computer system and the chassis, wherein the chassis comprises connector coupled to a switched fabric bus (InfiniBand) (at least Figs. 1-2 and pages 33-

36 and 54). However, InfiniBand Spec does not explicitly disclose the chassis being an instrumentation chassis comprising: a plurality of slots, wherein each of the plurality of slots is operable to receive an inserted module; a backplane, comprising: a plurality of instrumentation signaling lines which provide instrumentation signaling functions; a plurality of interface connectors coupled to the switched fabric bus and to the plurality of lines, wherein each of the connectors is operable to connect to a respective inserted module; wherein the backplane is operable to provide for communication among the inserted modules. PXI Spec teaches instrumentation chassis comprising: a plurality of slots (peripheral slots), wherein each of the plurality of slots is operable to receive an inserted module; a backplane (backplane), comprising: a plurality of instrumentation signaling lines which provide instrumentation signaling functions (Figure 2.4); a plurality of interface connectors coupled to the plurality of lines, wherein each of the connectors is operable to connect to a respective inserted module; wherein the backplane is operable to provide for communication among the inserted modules (Section 2.1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement instrumentation chassis as taught by PXI Spec to provide instrumentation functions in the system of InfiniBand Spec.

As to claim 36, PXI Spec further teaches the plurality of instrumentation signaling lines include one or more of: a local bus (Section 2.2.2); system reference clock signals (Section 2.2.3); a trigger bus (Section 2.2.4); and a star trigger bus (Section 2.2.5).

As to claim 37, PXI Spec further teaches the plurality of instrumentation signaling lines include one or more of: a local bus; system reference clock signals; a trigger bus; a

star trigger bus; a low voltage analog bus; and a high voltage analog bus. (Sections 2.2.2-2.2.5 and 4.1.2.5).

As to claim 38, InfiniBand Spec further teaches the switched fabric bus is a channel based switched fabric bus (IniniBand) (Specification).

As to claim 39, InfiniBand Spec further teaches the channel based switched fabric bus is the InfiniBand bus (Specification).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses instrumentation system:

US Patent	6,629,181	Alappat et al.
US Patent	6,640,273	Spisak et al.
US Patent	6,704,830	Spisak et al.
US Patent	5,619,722	Lovrenich
US Patent	6,397,286	Chatenever et al.
US Patent	6,442,639	McElhattan et al.
US Patent	6,351,786	Elmore et al.
US Patent	6,715,023	Abu-Lebdeh et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha U. Vu
Examiner
Art Unit 2112

uv

Sumati Lefkowitz

SUMATI LEFKOWITZ
PRIMARY EXAMINER